REMARKS

In the Office Action dated July 14, 2005, claims 1-3, 7, 8, 10-13, and 24-27 were rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,804,144 (Iwata); and claims 9, 15, 16, and 19-21 were rejected under § 103 over Iwata.

Applicant acknowledges the indication that claims 4-6, 14, 17, 18, 22, 23, 28, and 29 would be allowable if rewritten in independent form.

Claim 1 has been amended to substantially incorporate the substance of the subject matter recited in claims 2-4 (now cancelled). It is respectfully submitted that claim 1 is therefore now in condition for allowance.

Claims 6, 17, 22, and 28 have been amended from dependent form to independent form. These claims are therefore in condition for allowance.

Independent claim 15 has been amended to recite that each group of memory cells includes memory cells connected in parallel between a bias signal and a common node, and each group further comprises a transistor coupled between the common node and a respective bit line. In Iwata, the arrangement of memory cells in Figs. 3 and 17 (specifically cited by the Office Action) do not disclose provision of a transistor in each group being *between* the common node and a respective *bit line*. As indicated in the Office Action, a column depicted in Fig. 3 or Fig. 17 corresponds to a "group." In this group, the memory cells are directly connected between the bit line and another node (VSS in Fig. 3 and the drain of a transistor in Fig. 17). Neither the arrangement of Fig. 3 nor Fig. 17 depicts or suggests a transistor between a common node and the respective bit line. Therefore, claim 15 is allowable over Iwata.

Amended independent claim 24 is not disclosed by Iwata. Amended claim 24 recites selecting at least one of the plurality of groups of memory cells, where the memory cells comprise magnetoresistive elements, and where each group of memory cells includes a first set of memory cells connected in parallel between a first bias signal and a common node, and a second set of memory cells connected in parallel between a second bias signal and the common node. Moreover, the method of claim 24 recites setting the first and second bias signals of the selected group of memory cells at *different voltage potentials*.

The Office Action identified the first and second bias signals as being VSS in Fig. 17. Note that VSS is a ground potential, and therefore cannot satisfy the element in claim 24 of setting the first and second bias signals of the selected group of memory cells at *different* voltage potentials. Therefore, claim 24 is not anticipated by Iwata.

Newly added independent claim 30 is also similarly allowable over Iwata, which fails to disclose first and second bias signals set at different voltage potentials for a selected one of the groups of memory cells.

Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 08-2025 (200312363-1).

Respectfully submitted,

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